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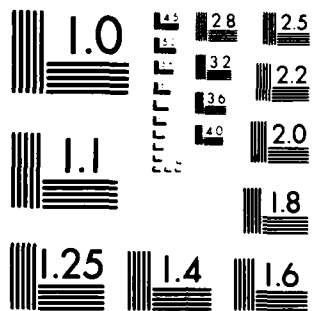
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COMBINED ENVIRONMENT TESTING OF TERMINAL PROTECTION DEVICES CONJOINED WITH BASIC INTEGRATED CIRCUITS

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22 May 1981

Final Report for Period 15 July 1978-30 April 1981

CONTRACT No. DNA 001-78-C-0344

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1 REPORT NUMBER DNA 5773F	2 GOVT ACCESSION NO. A122 210	3 RECIPIENT'S CATALOG NUMBER
4 TITLE (and Subtitle) COMBINED ENVIRONMENT TESTING OF TERMINAL PROTECTION DEVICES CONJOINED WITH BASIC INTEGRATED CIRCUITS	5 TYPE OF REPORT & PERIOD COVERED Final Report for Period 15 Jul 78 — 30 Apr 81	
7 AUTHOR Philip S. Book	6 PERFORMING ORG. REPORT NUMBER K-81-36U(R)	
9 PERFORMING ORGANIZATION NAME AND ADDRESS Kaman Sciences Corporation P. O. Box 7463 Colorado Springs, Colorado 80933	8 CONTRACT OR GRANT NUMBER(s) DNA 001-78-C-0344	
11 CONTROLLING OFFICE NAME AND ADDRESS Director Defense Nuclear Agency Washington, D. C. 20305	10 PROGRAM ELEMENT PROJECT TASK AREA & WORK UNIT NUMBERS Subtask Z99QAXTE501-07	
14 MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	12 REPORT DATE 22 May 1981	
	13 NUMBER OF PAGES 86	
	15 SECURITY CLASS. (of this report) UNCLASSIFIED	
	15a DECLASSIFICATION DOWNGRADING SCHEDULE N/A since UNCLASSIFIED	
16 DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		
17 DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18 SUPPLEMENTARY NOTES This work was sponsored by the Defense Nuclear Agency under RDT&E RMSS Code B323078464 Z99QAXTE50107 H2590D.		
19 KEY WORDS (Continue on reverse side if necessary and identify by block number) System-Generated Electromagnetic Pulse (SGEMP) Transient-Radiation Effects in Electronics (TREE) Semiconductor Burnout Combined Environment Effects Synergistic Effects		
20 ABSTRACT (Continue on reverse side if necessary and identify by block number) The objectives of this program were to develop an experimental method and conduct a series of tests to evaluate the effectiveness of terminal protection devices in a combined conducted current and ionizing radiation environment. An essential requirement of the test effort was to include a statistically signifi- cant number of test samples. A pulser design comprised of a charged coaxial line and a radiation-triggered SCR switch was selected. This design was assembled into a 4-channel configuration which was used to conduct combined environment tests at DNA's Blackjack 3 facility		

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20. ABSTRACT (Continued)

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This facility provided a prompt dose of about 3500 rads(Si) in the test circuits, and about 750 rads(Si) in the radiation-triggered pulser.

The test program encompassed 176 samples of the same type integrated circuit in various test configurations. For tests without terminal protection devices in place, the results indicate that current and power failure thresholds are slightly higher for a combined environment. Test results for configurations with terminal protection devices are somewhat incomplete because of the inability to induce a large number of failures. For the one configuration where a few failures were observed, test results indicate that terminal protection devices are more effective (by a current margin of 7 dB or greater) in a combined environment than for conducted current only.

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SUMMARY

Exposure of an electronic system to a high level exoatmospheric x-ray environment results in a simultaneous ionizing radiation and conducted current transient environment for some critical semiconductor pieceparts. Potentially harmful effects due to this combined environment have been investigated by previous experimental programs insofar as they pertain to individual pieceparts. The particular problem of concern for this program was investigation of combined environment effects on typical terminal protection devices that are incorporated into hardened designs to protect susceptible cable interface circuits.

One of the reasons for the paucity of combined environment data is the difficulty of providing a short current pulse in proper synchronization with a typical simulator prompt ionizing radiation pulse. This is an especially acute problem for the high current pulse amplitudes required to test terminal protection devices to expected failure levels.

The first of two program objectives was to select a technique and develop hardware to generate high-amplitude current pulses in near-coincidence with an ionizing radiation pulse. A multiple channel capability with each output up to 100A was desired in view of the anticipated test requirements. The second objective of this program was to conduct an experimental program to evaluate the effectiveness of terminal protection devices for conducted current only and in a combined environment. An essential requirement of the test effort was to include a statistically significant number of test samples.

A pulser design comprised of a charged coaxial line and a radiation-triggered SCR switch was selected. This design was assembled into a 4-channel configuration; it provided up to 100A on each channel, or a peak amplitude of approximately 400A via appropriate

summing of individual outputs. A similar charged-line design but with a conventional spark gap switch was used for the laboratory testing without simultaneous ionizing radiation.

A simple terminal protection network in conjunction with a basic TTL integrated circuit was selected as the test article. Eighty units in eight different test arrangements were subjected to current step-stress testing in KSC laboratory facilities, and ninety-six units in the same eight test arrangements were subjected to combined environment testing. The combined environment tests were conducted at DNA's Blackjack 3 facility which provided a prompt dose of about 3500 rads(Si) in the test circuits, and about 750 rads(Si) in the radiation-triggered pulser.

For test integrated circuits without terminal protection devices in place, the results indicate that current and power failure thresholds are slightly higher for a combined environment than for conducted current only. The results also show a very close grouping of failure thresholds which is probably due to purchase of test integrated circuits with the same manufacturer's date code.

Test results for configurations with terminal protection devices are somewhat incomplete because of the inability to induce a large number of failures. For the one configuration (negative polarity test pulses on the integrated circuit input terminal) where a few failures were observed, test results indicate that terminal protection devices are more effective (by a current margin of 7 dB or more) in a combined environment.

Based on the data developed from this program, it cannot be definitively concluded that terminal protection devices are more effective in a combined environment than for conducted current only. However, there are no data to indicate unexpected responses or interactions or otherwise suggest that terminal protection devices are less effective in a combined environment.

With respect to the experimental procedure, it is concluded that the radiation-triggered charge-line pulser is a viable design approach.

The necessity for and precise direction of future combined environment test work is not well-defined. It is clear, however, that test circuit parasitics are important and perhaps dominant contributors to observed responses. Therefore, test programs directed towards specific system questions should be conducted with test articles very similar to final hardware configurations.



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PREFACE

This report was prepared by Kaman Sciences Corporation (KSC) under contract DNA001-78-C-0344.

The author expresses his appreciation to Mr. Louis Ortiz for assembly of test apparatus, conduct of all in-house tests and participation in the field tests at DNA's Blackjack 3 facility. Thanks are also due to Mr. John Farber and LCDR Bill Mohr of DNA who arranged for the use of Blackjack 3, and Maxwell Laboratories, Inc. personnel who provided the test services in a timely manner.

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COMBINED ENVIRONMENT TESTING OF TERMINAL PROTECTION DEVICES CONJOINED WITH BASIC INTEGRATED CIRCUITS

SECTION 1.0

INTRODUCTION

1.1 BACKGROUND AND OBJECTIVES

Military satellite and missile systems are required to withstand exposure to high level exoatmospheric x-ray environments without incurring permanent functional degradation. X-ray interactions with system cables and other structures induce current transients which are conducted into semiconductor devices via cables which interface various electronic subsystems. In near-coincidence with generation of these conducted transients, the x-rays ionize the semiconductor pieceparts. This combination of conducted current transient and simultaneous ionizing radiation is commonly referred to in this report and throughout the technical literature as the "combined environment".

Under certain conditions, the conducted transients can be of sufficient magnitude so as to permanently damage semiconductor pieceparts connected to termination points of interconnecting cables. The most common approach to hardening against conducted transients is to employ terminal protection devices (TPDs) near cable terminations to prevent damage to susceptible semiconductor pieceparts. Large area Zener or avalanche diodes especially designed for very high surge current operation are the most common type of TPD. These devices are typically used in a configuration which shunts most of the current transient to ground and limits the terminal voltage to a value near the breakdown voltage rating of the TPD. Given the failure parameters of a sensitive piecepart and the surge current characteristics of various types of TPDs, a designer can configure a specific design to achieve a certain margin relative to a specified terminal threat.

A potentially significant weakness inherent to this design approach is that piecepart failure parameters and TPD surge current characteristics are usually based on laboratory tests performed without the simultaneous ionizing radiation environment that is characteristic of the actual threat. It is possible that ionizing radiation could affect the piecepart failure parameters, the characteristics of the TPD, or the current distribution between the two devices in a manner that would result in a design margin considerably less than expected.

The objectives of this test and data analysis program were to develop a suitable experimental procedure and to evaluate the effectiveness of TPDs in a combined transient current and ionizing radiation environment. An effectiveness criterion of specific interest is the design margin for an actual combined environment in comparison to the design margin based on test data and other design considerations for conducted current alone.

1.2 SCOPE OF REPORT

Section 2 of this report is a more detailed description of the technical problem of particular interest for this program. This discussion provides further problem background information and establishes the framework for the experimental approach, laboratory tests and combined environment tests described in Sections 3, 4 and 5, respectively. Tabulated raw data and results of limited statistical analyses are presented in Section 6. Conclusions from this program and recommendations for future work of a similar nature are given in Section 7.

SECTION 2.0

TECHNICAL DISCUSSION

2.1 COMBINED ENVIRONMENT EFFECTS

The combined environment problem addressed by this program can best be understood from a brief review of the important elements and design considerations for a simple hardened cable termination. Figure 1 is a block diagram of such a termination; this diagram depicts the conducted current threat, I_c , injected into a hardened termination comprised essentially of a rugged TPD network, one or more pieceparts (usually semiconductors) typically susceptible to burnout at a comparatively low current level (1 to 5A), and parasitic impedances Z_1 and Z_2 . The normal design approach is to use an established piecepart failure model of the form

$$P_F = kt^{-1/2} \quad (1)$$

and calculate I_F from the quadratic equation

$$I_F = \frac{-V_{BD}^2 + \sqrt{V_{BD}^2 + 4R_S P_F}}{2R_S} \quad (2)$$

and V_F from the simple expression

$$V_F = P_F / I_F \quad (3)$$

where P_F is failure power for a rectangular pulse,

t is width of rectangular pulse equivalent of actual threat waveform,

k is a piecepart failure constant obtained from test data or derived from estimation algorithms,

V_{BD} is breakdown voltage of most sensitive junction within the piecepart,

R_S is junction surge resistance.

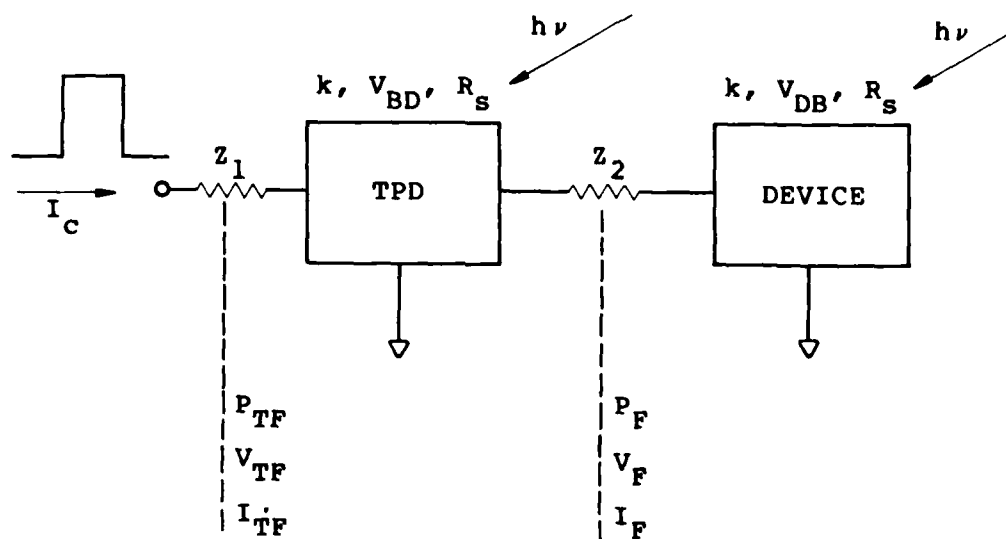


Figure 1. Block diagram of hardened termination.

Based on these calculated values of I_F and V_F and the interface functional requirements, a designer must configure a TPD network such that the terminal power or current, P_{TF} or I_{TF} , required to cause piecepart failure is well above the terminal threat. At the same time, he must assure that the TPD itself can withstand a worse case terminal threat. The degree of success achieved by this effort is usually expressed as a design margin, DM, which is defined by *

$$DM = 20 \log \frac{I_{TF}}{I_{Threat}} \quad (4)$$

* For the purposes of this report, DM is defined in terms of current (rather than power) because of the impracticality of calculating terminal power for test configurations wherein the defined-terminal voltage is limited to a low value.

For the most part, the design approach outlined above has been undertaken with only minimal consideration for possible effects due to simultaneous ionizing radiation. In general there are two types of effects which could cause the design margin to be less than expected. First of all, ionizing radiation could cause a decrease in the piecepart or TPD failure threshold which clearly would lower the design margin. A second, more subtle, effect is that ionizing radiation could cause other semiconductor parameters to change in such a way as to result in a different-from-expected current distribution between the susceptible piecepart and TPD.

The possibility of a reduced piecepart burnout failure threshold due to the presence of ionizing radiation simultaneously with a conducted transient is the problem area that has historically been referred to as the synergistic effects problem. Several experimental programs have been carried out to examine synergistic effects in discrete pieceparts.^{1,2,3,4} The consensus from these efforts is that an ionizing radiation environment does not cause a significant change in pulse burnout failure thresholds. This conclusion supports intuitive arguments which postulate that ionizing radiation could increase tolerance to pulse current by preventing or relieving current constriction sites which lead to burnout.

Reference 5 reports on an experimental program designed to investigate synergistic effects at the circuit level. The thesis underlying that work was that ionizing radiation could result in current paths and associated damage modes different from those encountered from pulse testing in the absence of a radiation environment. Although the experiment design allowed for current distribution among multiple paths, it did not include a TPD as one of the alternative current paths. The report concluded that circuit failure thresholds (for the combined environment) appear to be no lower than those for laboratory tests with injected current pulses only; this overall conclusion is somewhat indefinite because of the limited scope of the effort and difficulty of the experimental problem.

2.2 EXPERIMENTAL PHILOSOPHY

This program was undertaken to expand the combined environment data base by testing a statistically significant number of samples of several representative types of cable termination circuit. In an experimental program where the test articles and test variables are not well-defined, somewhat subjective decisions must be made in regard to what constitutes a meaningful but manageable effort within program time and funding constraints. The following paragraphs summarize the major elements of this experimental program.

2.2.1 Circuit Configurations

Figure 2 shows the test configurations which were selected for evaluation. The 54L04 inverter circuit is the simplest integrated circuit (IC) that might be used in a line driver or line receiver application; however, it is representative of the very broad class of TTL logic that employs a TTL input and totem pole output. The terminal protection network consists of Zener diode CR1 and resistor R1; this is one of the simplest forms of terminal protection and is based on design guidelines given in Reference 6.

Each of the four configurations was subjected to laboratory* tests and combined environment tests with both positive and negative polarity 100 ns pulses. Testing was initiated at a pulse amplitude below the expected burnout threshold and increased in a step-wise manner (a factor of 2 or 3 each step) until all samples were failed or until the upper limit of the pulser was reached.

* The term "laboratory tests" is used to distinguish the baseline pulse tests from the combined environment tests.

INSTRUMENTATION/TEST CIRCUIT INTERFACE

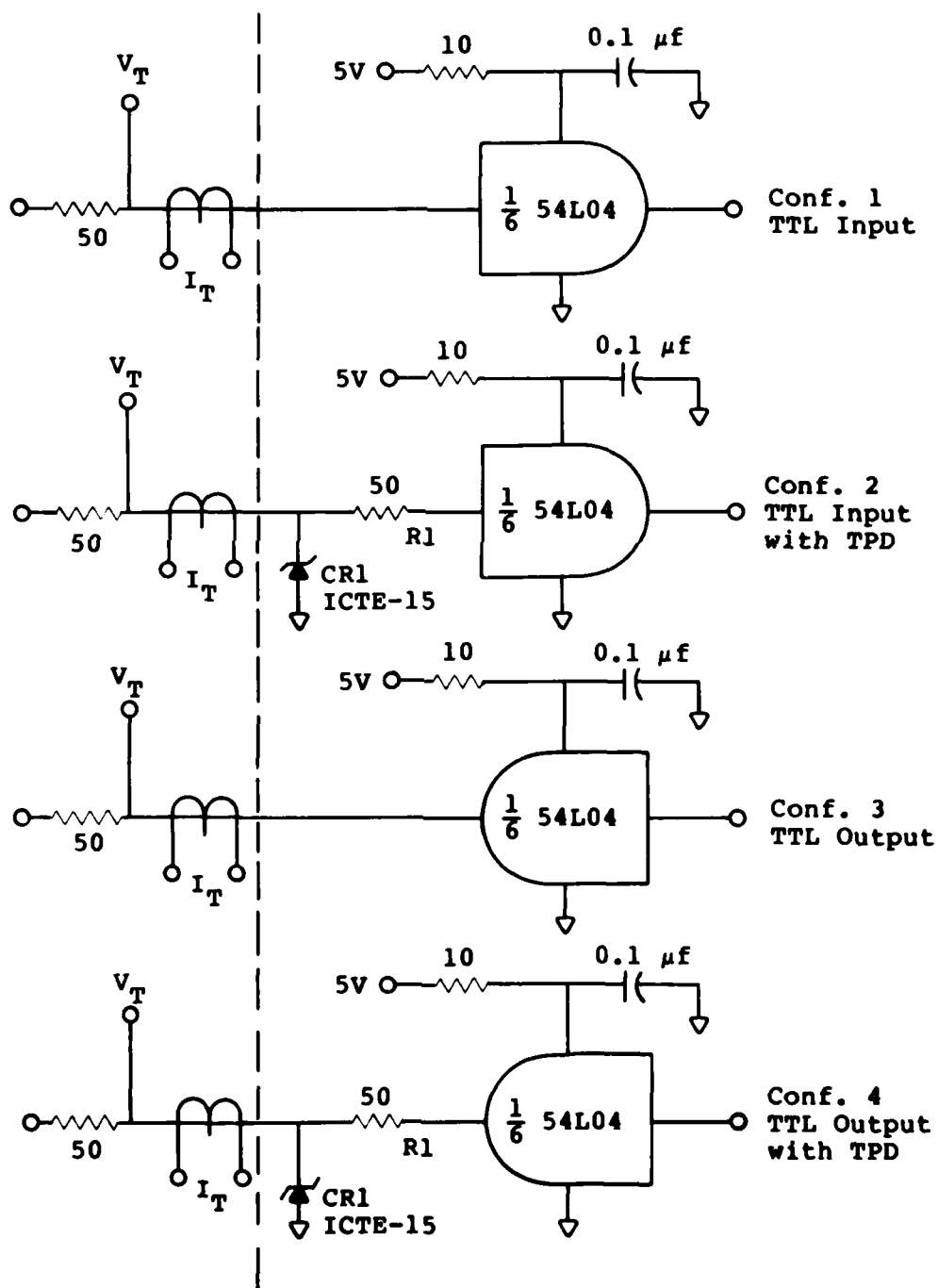


Figure 2. Test configurations for combined environment testing.

2.2.2 Data Requirements

As noted previously, the overall program objective was to evaluate the effectiveness of TPDs in a combined environment. This requires data for four part sets* for each test configuration in order to make the following determinations:

- (a) Piecepart failure threshold, P_F or I_F , for laboratory tests.
- (b) Piecepart failure threshold for combined environment tests.
- (c) Terminal power or current, P_{TF} or I_{TF} , required to cause piecepart failure for laboratory tests with TPD in place.
- (d) Terminal power or current required to cause piecepart failure for combined environment tests with TPD in place.

Given the data base indicated above, there are several ways to evaluate TPD effectiveness. The criterion of most interest is actual design margin in the combined environment [based on results from (a) and (d) tests] relative to the design margin expected from laboratory test data [based on results from (a) and (c) tests]. The operable definition of design margin is

$$DM = 20 \log \frac{I_{TF}}{I_{Threat}}, \quad (5)$$

or in terms of combined environment versus laboratory,

$$DM(\gamma \neq 0) - DM(\gamma = 0) = 20 \log \frac{I_{TF}(\gamma \neq 0)}{I_{TF}(\gamma = 0)}. \quad (6)$$

The purpose of data sets (a) and (b) is to provide a basis to determine if observed differences in design margin are attributable to ionization-induced variations in piecepart failure thresholds or current redistribution due to ionization.

* Positive and negative polarity test pulses for both laboratory and combined environment tests.

It is well-known that burnout thresholds are subject to wide statistical variation. To minimize uncertainty due to this type of part-to-part variation, a sample size of either 10 or 12 was used for each of the 16 part sets. In addition, all parts were from the same production date code.

2.2.3 Current and Radiation Level Requirements

A considerable amount of pulse test data has been published⁷ for discrete semiconductor pieceparts and integrated circuits. This requires a test capability of 1-10A which is relatively easy to achieve. However, it was recognized early in the program that test circuits configured with TPDs might survive very high pulse levels, and that testing to failure would be a formidable task. The goal was to provide a 100A test capability (compatible with other experimental requirements) for both the laboratory and combined environment tests, and test to failure or pulser limit whichever occurred first.

There is no firm radiation level requirement for this type of combined environment testing. Different systems will have different prompt dose requirements depending on threat and x-ray shielding of TPDs and pieceparts. Moreover, there is no assurance that the maximum system dose will be the worse case for the effects of interest. There is, of course, a minimum prompt dose requirement on the order of several kilorads(Si) to assure complete ionization of the TPD and/or piecepart under test.

SECTION 3.0

EXPERIMENTAL PROCEDURE

3.1 LABORATORY PULSERS

Laboratory pulse tests were performed with two different pulser. A Paravan Model 1500 was used for those test configurations which did not include a TPD. The Model 1500 is a charged-line pulser employing a mercury-wetted reed relay switch. It provides a variable width (depending on length of charge line) positive or negative pulse up to 20A into a 50-ohm load; rise and fall times are typically less than 1 ns.

For those test configurations which did include a TPD, a much higher amplitude pulse capability was required. A charged-line pulser employing a hermetically sealed triggered spark gap (EG&G Model GP-20B) was designed and fabricated in the Kaman laboratory. This pulser provides a positive or negative pulse up to 100A into a 50-ohm load; pulse width is fixed at 100 ns and rise and fall times are 10-15 ns depending somewhat on pulse amplitude. This design approach can be extended to provide a much higher pulse amplitude but care must be taken to guard against voltage breakdown of pulse transmission cables and other marginal insulation paths.

3.2 COMBINED ENVIRONMENT PULSER

Theoretical considerations and previous experimental work indicate that circuit-level combined environment effects are likely to be most significant if the semiconductors are ionized before the arrival of the conducted current pulse. It is argued that this scenario represents worse case since it allows for the possibility of a current distribution most different from that due to a conducted current pulse only. The significance of this concept from an experimental viewpoint

is that the leading edge of the ionizing radiation pulse should precede the leading edge of the injected current pulse by 10 to 20 ns. This synchronization requirement and the pulse amplitude requirement are driving factors in the selection of a suitable pulsing technique.

Compton diode, coaxial cable SGEMP effects, charged coaxial cable with a radiation-triggered spark gap switch, flash x-ray machine and pulser synchronization from a common trigger, and charged coaxial cable with a radiation-triggered SCR switch are some of the pulsing techniques which were considered. Reference 5 and this program concluded that a charged line with a radiation-trigger SCR switch was the best approach to satisfy the current pulse amplitude and synchronization requirements most reliably. The design developed and used for this program is shown in Figure 3. It provides four separate 100 ns output pulses with an amplitude range from 5 to 100A. Radiation testing and analysis experience suggests that the SCR switches should be uniformly irradiated to about 1 krad(Si) to effect the very fast switching necessary to generate the output current pulses within 10 to 20 ns from the leading edge of the ionizing radiation pulse. Note that this required performance is much faster than the normal gate-controlled turn-on time which is specified as 1-3 μ s for the 2N6399 type SCR. Either polarity output pulses can be obtained by appropriate orientation of the SCR stacks and selection of charging supply polarity.

Figures 4 and 5 are photographs of the SCR stacks (including grading resistors) and overall pulser assembly, respectively. Typical pulser performance in the Blackjack 3 test series (described in detail in Section 5) is illustrated in Figure 6; the upper trace in each photograph shows the radiation pulse and the lower trace shows the current pulse input into one of the four test terminals. It is to be noted that approximately 50 percent of the prompt dose has been deposited (in the test piecepart and TPD) by the time the current pulse has increased to near its peak value.

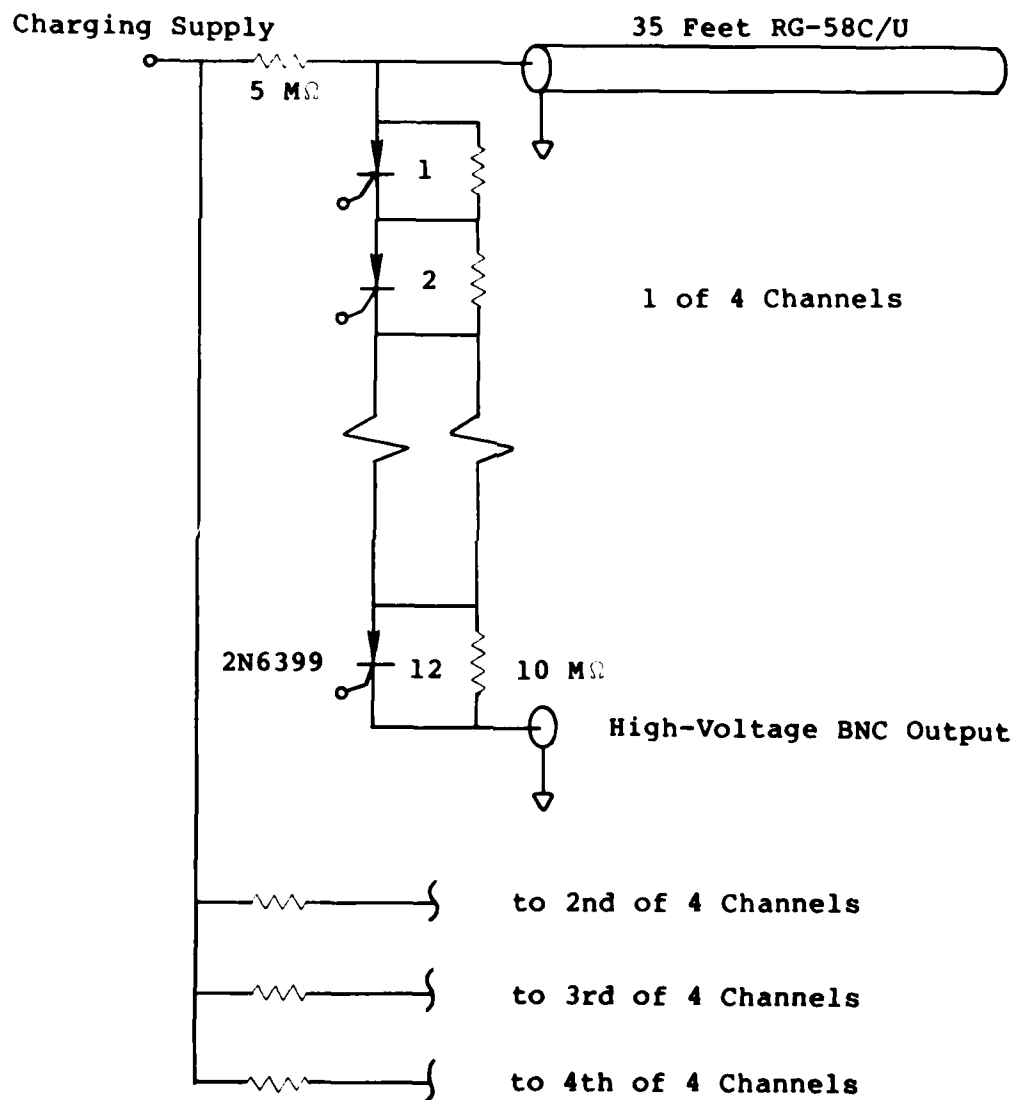
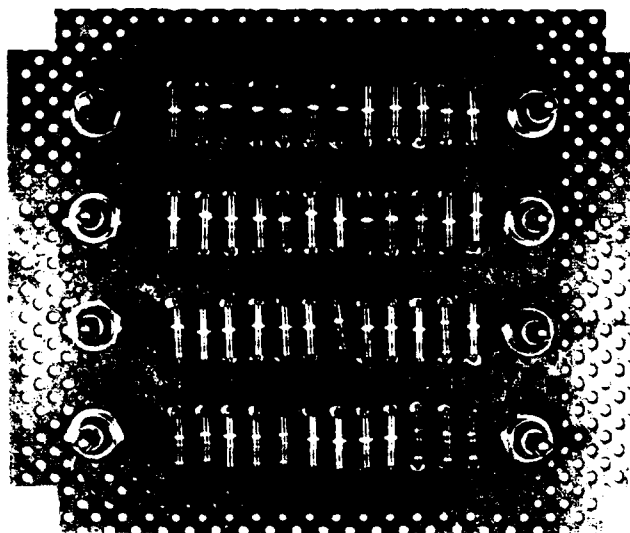
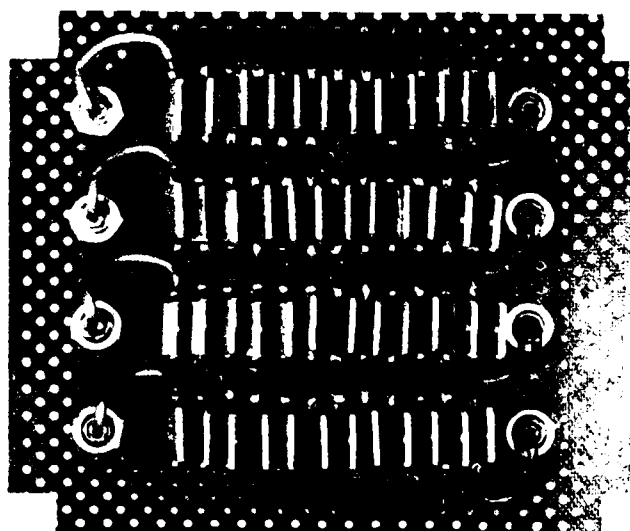


Figure 3. Schematic diagram of radiation-triggered charged-line pulser.



Grading
Resistor
Side



SCR
Switch
Side

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Figure 4. Photograph of high-voltage SCR switch assembly.

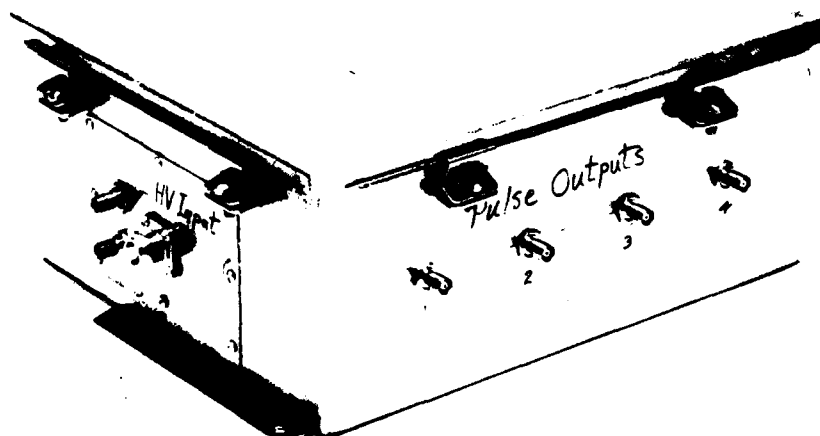
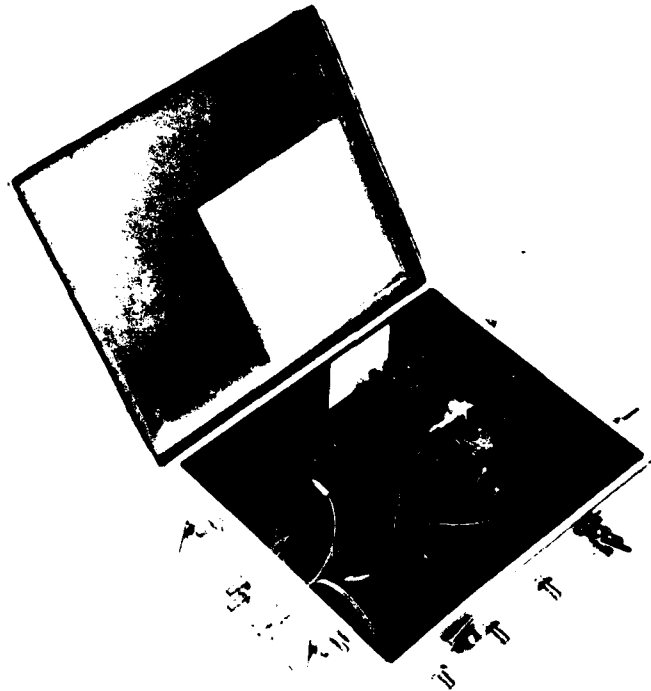
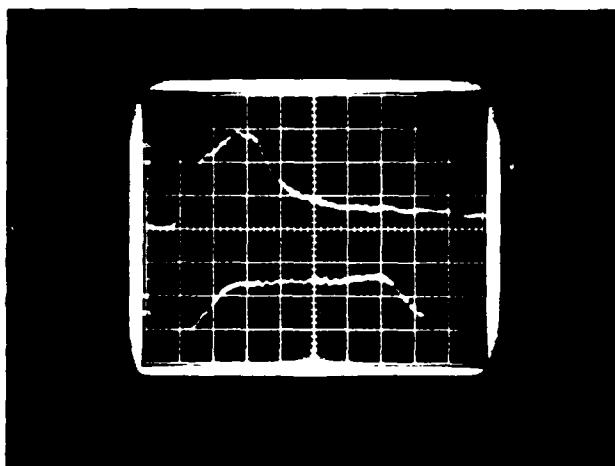


Figure 5. Complete radiation-triggered pulser as packaged in shielded enclosure.



Test Shot 3785

Upper Trace: Pin Current

S_V : 0.4 A/div

S_H : 20 ns/div

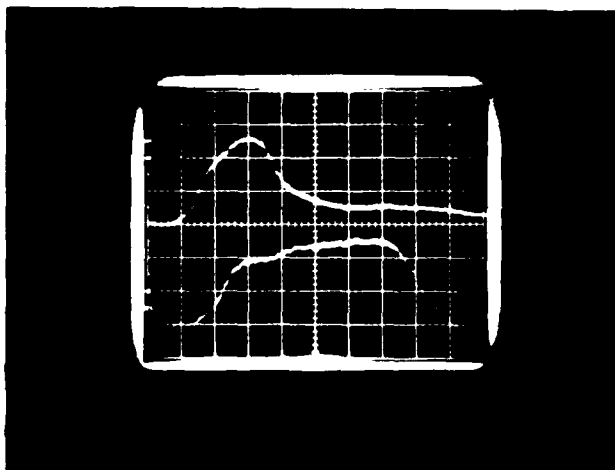
Lower Trace: Terminal 1 Current

S_V : 50 A/div

S_H : 20 ns/div

Remarks .

$V_{\text{Charge lines}} = 7 \text{ kV}$



Test Shot 3788

Upper Trace: Pin Current

S_V : 0.4 A/div

S_H : 20 ns/div

Lower Trace: Terminal 1 Current

S_V : 50 A/div

S_H : 20 ns/div

Remarks :

$V_{\text{Charge lines}} = 10 \text{ kV}$

Figure 6. Typical performance of radiation-triggered pulser.

One final aspect of the pulser design and assembly should be discussed. Some of the initial program planning had indicated that it might be necessary to delay the current pulses relative to the radiation pulse. This consideration influenced the pulser to be designed as a 50-ohm source and packaged in a separate enclosure such that delay cables could be inserted between the pulser and test devices. Although this capability was not used in the Blackjack 3 test series, it appears to be a generally useful design feature.

3.3 TEST INSTRUMENTATION

In general, test data must be sufficient to determine the occurrence of permanent functional degradation of any piecepart in the circuit under test and also, permit a reliable estimation of failure current or failure power. Figure 7 shows the basic sensing instrumentation used for both laboratory and combined environment tests. Included in this figure (identified by dashed lines) is a modified configuration used during the latter part of the Blackjack 3 test series. For the test configurations which did not include a TPD, resistor R1 was shorted and diode CR1 was removed. Figure 8 consists of photographs of the test package showing the overall enclosure, layout of four test circuits with current probes, and relatively close spacing of four test ICs.

The purpose of the basic instrumentation was to acquire terminal current and voltage data to enable calculation of power delivered into the terminal (clearly, with no TPD in place, terminal power is equivalent to power into the piecepart under test). Also, based on previous test experience and reported results from other burnout testing programs, it was initially believed that transient current and voltage data would indicate the precise time of failure (by a distinct discontinuity in current and/or voltage waveforms). In practice, neither the laboratory nor combined environment transient data manifested a reliable indication of failure time. Apparently, this is because

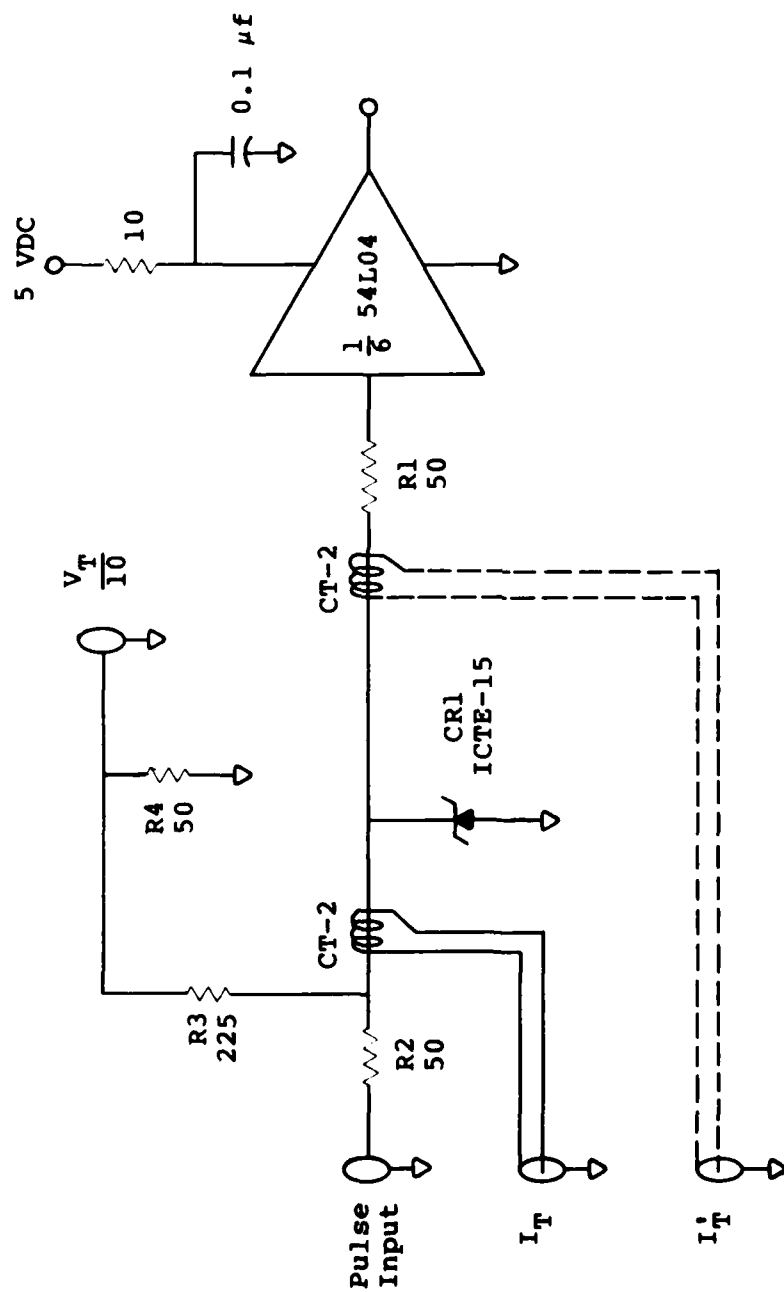
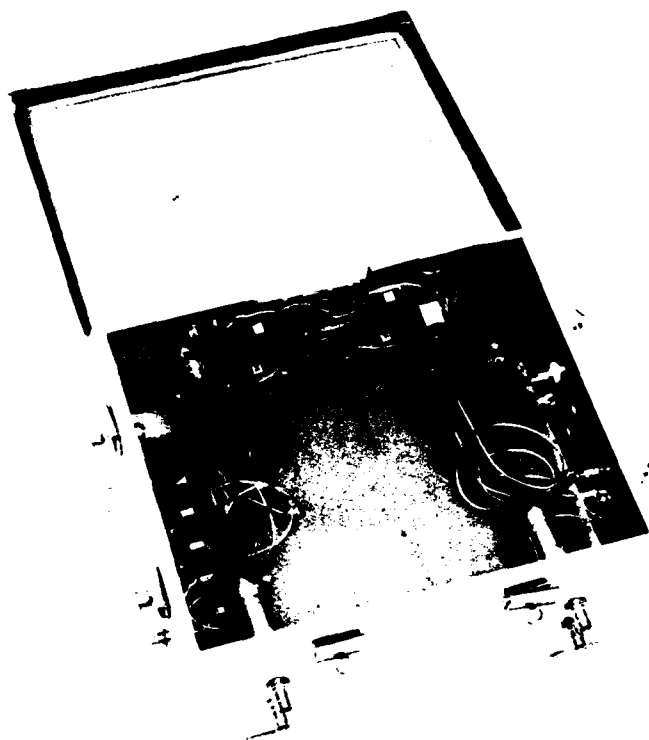
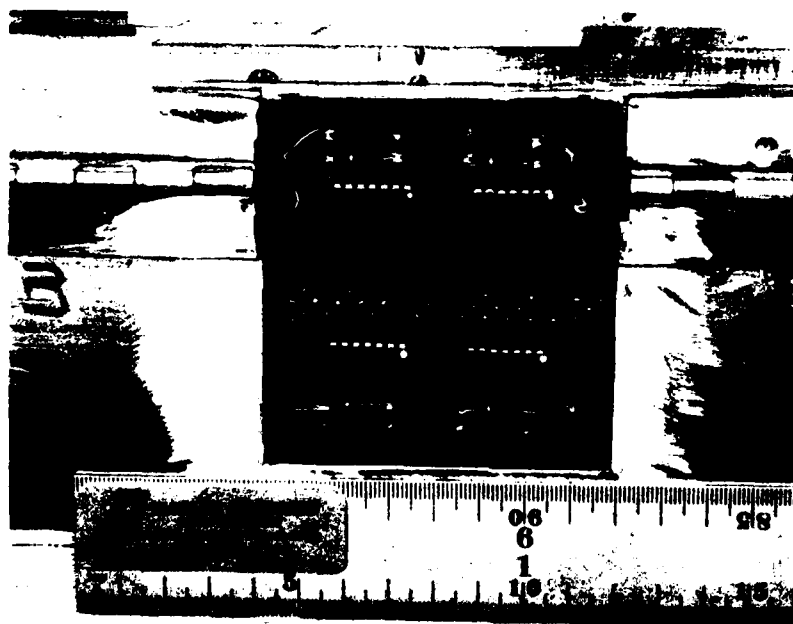


Figure 7. Schematic diagram of basic and modified test instrumentation.



Layout of Test
Circuits and
Current Probes



ICs in Test
Position Near
Enclosure
Window

Figure 8. Photographs of test circuit.

integrated circuit burnout involves multiple low-voltage junctions and current paths unlike a discrete piecepart which encompasses only one junction and one surge resistance term.

The absence of a dependable time-of-failure indicator has two implications from an experimental viewpoint; first, it means that the amplitude increments in the step-stress pulse sequence must be relatively small to obtain a fair degree of resolution in failure power or current; and second, it means that test ICs must be electrically characterized after each test pulse to determine the occurrence of functional degradation. Table 1 indicates the scope of data taken on each integrated circuit and TPD tested. A Beckman Model 999 portable integrated circuit tester and a Tektronix Model 575 curve tracer were used to make the measurements.

Table 1
Scope of electrical characterization measurements
for integrated circuits and TPDs.

PARAMETER	TEST CONDITION
High-level output voltage, V_{OH}	$V_{IL} = 0.7V$ $I_{OH} = 0.2 \text{ mA}$
Low-level output voltage, V_{OL}	$V_{IH} = 2.0V$ $I_{OL} = 2.0 \text{ mA}$
High-level input current, I_{IH}	$V_{IH} = 5.0V$ $V_{CC} = 5.0V$
Low-level input current, I_{IL}	$V_{IL} = \text{Ground}$

Reverse breakdown voltage, V_{R1}	$I_R = 1 \text{ mA}$
Reverse breakdown voltage, V_{R2}	$I_R = 50 \text{ mA}$

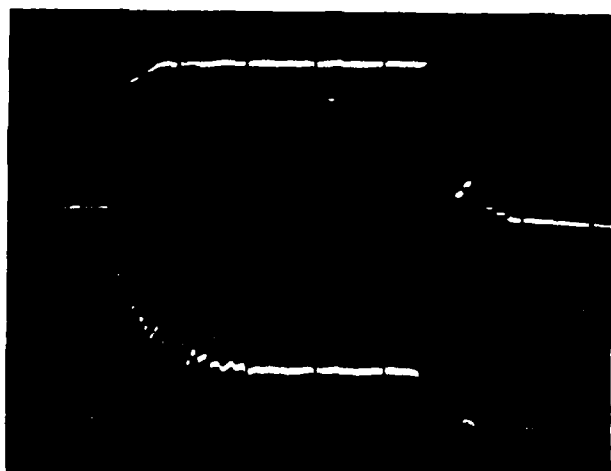
SECTION 4.0

LABORATORY TEST RESULTS

4.1 EXAMPLES OF DATA

Figures 9 and 10 are examples of typical laboratory data for positive test pulses applied to IC input terminals (refer to Figure 2 for details of test configurations). These data were recorded with a Tektronix Model 7844 oscilloscope equipped with a Model C-52 camera. Table 2 is a compilation of the electrical characterization data for the same two test units (SN 20 and SN 23) considered in Figures 9 and 10. Several features should be noted because of their importance to conduct of the experimental program and interpretation of test results:

- (1) All of the voltage waveform data show an inductive response at the pulse leading and trailing edges. This is due to parasitic inductance inherent to the test circuits; it is extremely difficult to achieve a transmission line test configuration and still provide for ready access and removal of test pieceparts for periodic electrical characterization. The inductive response is disquieting but probably not an important factor for this test program in view of the relatively wide current pulse. Approximate pulse power or energy can be calculated by simply neglecting the inductive component of the overall response.
- (2) Using known or measured values of pulser charge voltage, pulser source impedance (50 ohms), test circuit input impedance (also about 50 ohms), and terminal voltage, terminal current can be calculated with a reasonable degree of accuracy. This is significant in that it means that useful data can be obtained from a single transient measurement.



Unit SN 23

Test Pulse 004209

Upper Trace: Terminal Current

S_V : 2 A/div

S_H : 20 ns/div

Lower Trace: Terminal Voltage

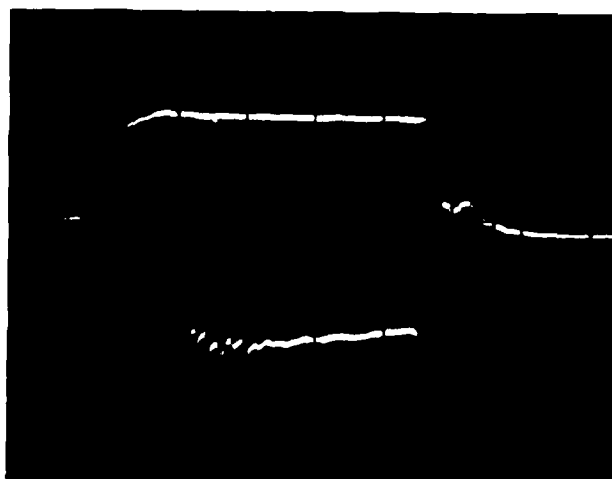
S_V : 45 V/div

S_H : 20 ns/div

Remarks.

Highest pass test level.

$V_{\text{Charge line}} = 480V$



Unit SN 23

Test Pulse 004210

Upper Trace: Terminal Current

S_V : 5 A/div

S_H : 20 ns/div

Lower Trace: Terminal Voltage

S_V : 45 V/div

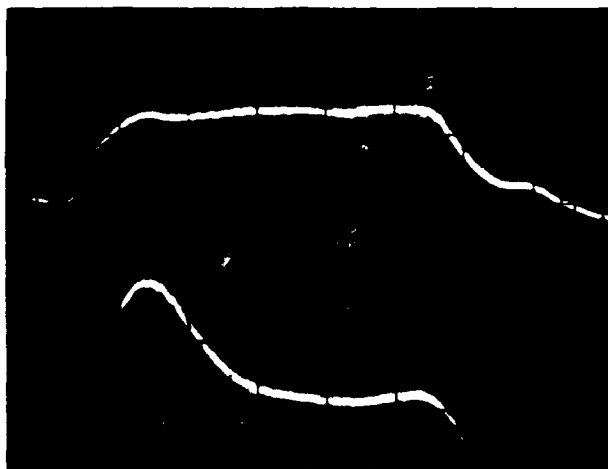
S_H : 20 ns/div

Remarks:

Failure test level.

$V_{\text{Charge line}} = 840V$

Figure 9. Typical data for pulse test without TPD.



Unit SN 20

Test Pulse 001823

Upper Trace: Terminal Current

S_V : 50 A/div

S_H : 20 ns/div

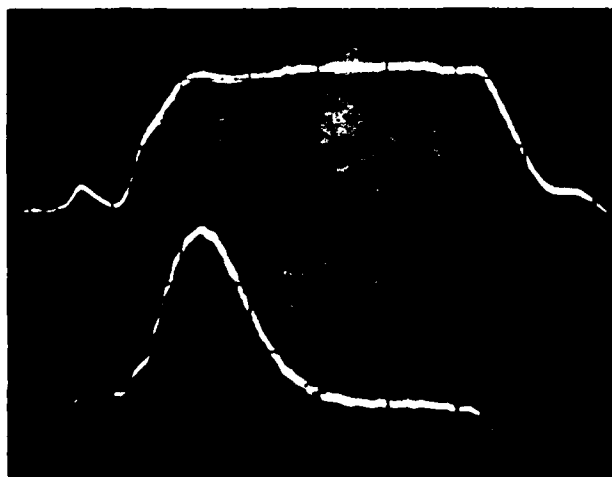
Lower Trace: Terminal Voltage

S_V : 180 V/div

S_H : 20 ns/div

Remarks:

$V_{\text{Charge line}}$ = 7 kV



Unit SN 20

Test Pulse 001824

Upper Trace: Terminal Current

S_V : 50 A/div

S_H : 20 ns/div

Lower Trace: Terminal Voltage

S_V : 180 V/div

S_H : 20 ns/div

Remarks:

Highest test level.

$V_{\text{Charge line}}$ = 10 kV

Figure 10. Typical data for pulse test with TPD.

- (3) The electrical characterization data presented in Table 2 clearly indicate that the unit under test experienced permanent damage due to test pulse number 004210. Observed changes in V_{OH} and V_{OL} are much greater than measurement uncertainties.
- (4) The two photographs included in Figure 9 bracket the true pulse failure threshold for integrated circuit SN 23. However, there is no clear indication in the lower set of transient data that failure has occurred. Consequently, the electrical characterization data must be relied on to provide positive indication of functional degradation.

An additional example of electrical characterization data is presented in Table 3. These data are for negative pulse testing of an IC input terminal protected by a TPD (configuration 2). The decisive point is the small but significant change in I_{IL} at the 120A pulse level; this is hypothesized to be a positive indicator of the permanent damage threshold for this unit. The hypothesis is reinforced by the more apparent change in I_{IL} at a subsequent lower level current pulse. Figure 11 shows the transient data for the 120A and 100A test pulses of special interest. These data were taken with the modified instrumentation configuration shown in Figure 7 in order to measure current into the test IC as well as terminal current per se. The observed peak current value of approximately 3A is indeed within the expected failure range. Therefore, based on the specific evidence cited and overall program test experience, it is concluded that some ICs protected by TPDs did experience permanent damage, and the permanent damage threshold was usually manifested by a small change in I_{IL} . This criterion for permanent damage is used in following data tabulations and summaries.

Table 2
Electrical characterization data for test
units SN 20 and SN 23.

IC SN	PULSE AMPLITUDE (A)	PULSE NUMBER	POSTPULSE PARAMETER VALUE			
			V _{OH} (V)	V _{OL} (V)	I _{IH} (μ A)	I _{IL} (mA)
20	Prepulse	NA	3.37	0.095	1.4	0.108
20	20	001821	3.33	0.095	1.5	0.109
20	40	001822	3.33	0.095	1.5	0.110
20	70	001823	3.33	0.095	1.4	0.110
20	100	001824	3.34	0.094	1.5	0.109
23	Prepulse	NA	3.27	0.081	1.1	0.120
23	2	004208	3.34	0.085	1.1	0.120
23	4	004209	3.38	0.085	1.2	0.120
23	7	004210*	2.75	0.102	1.1	0.120

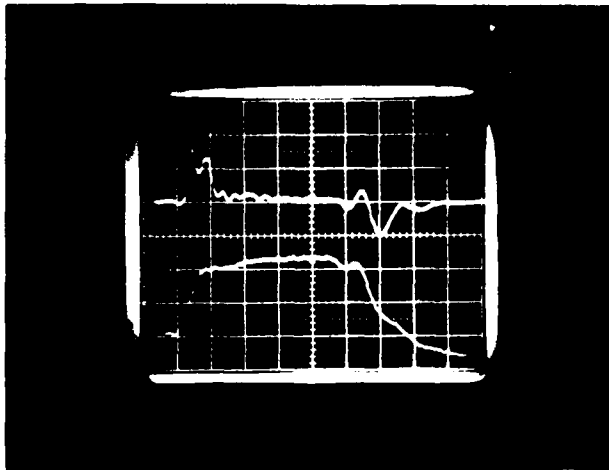
* Most device parameters indicate permanent damage due to this pulse.

Table 3
Electrical characterization data for test
unit SN 181.

IC SN	PULSE AMPLITUDE (A)	PULSE NUMBER	POSTPULSE PARAMETER VALUE			
			V _{OH} (V)	V _{OL} (V)	I _{IH} (μ A)	I _{IL} (mA)
181	Pretest	NA	3.30	0.094	0.4	0.117
	40	109101	3.30	0.094	0.4	0.117
	70	109102	3.31	0.094	0.4	0.117
	100	109103	3.31	0.094	0.4	0.117
	120	109104	3.24	0.093	0.4	0.121*
	70	109105	3.28	0.093	0.4	0.113
	100	109106	3.27	0.081	0.8	0.484**

* Indication of permanent damage threshold.

** Confirmation of permanent damage.



Unit SN 181

Test Pulse 109104

Upper Trace: IC Current

S_V : 2 A/div

S_H : 20 ns/div

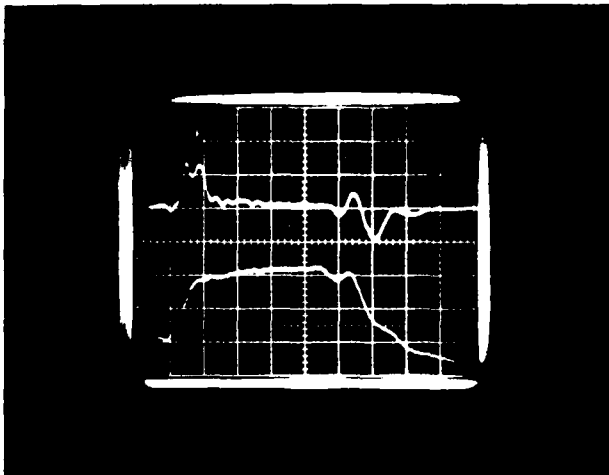
Lower Trace: Terminal Current

S_V : 50 A/div

S_H : 20 ns/div

Remarks:

$V_{\text{Charge line}} = -12 \text{ kV}$



Unit SN 181

Test Pulse 109106

Upper Trace: IC Current

S_V : 2 A/div

S_H : 20 ns/div

Lower Trace: Terminal Current

S_V : 50 A/div

S_H : 20 ns/div

Remarks:

$V_{\text{Charge line}} = -10 \text{ kV}$

Figure 11. Transient data for test unit SN 181.

The permanent damage threshold defined in the preceding paragraph might also be referred to as an "incipient failure" threshold. The increased value of I_{IL} measured subsequent to pulse number 109104 was still well within the specified maximum of 0.180 mA such that this unit did not experience true functional failure at this pulse level. However, at a somewhat lower amplitude pulse later in the test sequence, the unit did experience true failure with respect to specified electrical characteristics.

4.2 DATA SUMMARY

Tables 4-11 are summaries of laboratory transient data for the ten samples of the eight test groups (positive and negative pulse testing of four test configurations). As noted in the preceding section in the discussion of typical data, the "highest pass level" and "lowest failure level" pertain to the successive pulses which bracket the true failure threshold. Obviously, there are no data entries in the "lowest failure level" columns where the 100A laboratory pulser limit was insufficient to cause IC or TPD damage. The current and voltage values given in Tables 4-11 are simple "eyeball" averages of oscilloscope data (such as that illustrated in Figures 9 and 10) wherein obvious inductive contributions have been excluded from the averaging procedure; average resistance and average power are merely the quotient and product of average voltage and average current, respectively. More accurate operations on transient data are not deemed useful in view of the coarse resolution of failure threshold, or necessary because of the intended purposes for the data.

Table 4
Summary of laboratory test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
Cl; positive pulse on TTL input.	01	001501	2.0	76	38	152	001502	4.2	117	29	491
	02	001505	2.0	80	40	160	001506	4.6	115	25	529
	03	001507	2.0	85	42	170	001508	4.2	135	32	567
	04	001509	2.0	85	42	170	001510	4.0	135	34	540
	05	001512	4.2	140	33	588	001513	13	220	17	2860
	06	001514	2.0	85	42	170	001515	4.3	120	28	516
	07	001602	4.0	144	36	576	001603	7.5	190	25	1425
	08	001605	4.0	120	30	480	001606	8.0	170	21	1360
	09	001607	2.0	80	40	160	001608	4.3	115	27	495
	10	001610	4.2	117	28	491	001611	7.5	180	24	1350

Table 5
Summary of laboratory test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C2; positive	11	001704	100	35							
pulse on TTL	12	001708	100	35							
input with	13	001712	100	35							
TPD in place.	14	001716	100	35							
	15	001804	100	35							
	16	001808	100	35							
	17	001812	100	35							
	18	001816	100	35							
	19	001820	100	35							
	20	001824	100	35							

Table 6
Summary of laboratory test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C3; positive	21	003903	4.1	37	9.0	152	003904	5.4	41	7.6	221
pulse on TTL	22	004204	5.4	38	7.0	205	004205	7.0	42	6.0	294
output.	23	004209	4.2	32	7.6	134	004210	7.4	59	8.0	437
	24	004213	7.7	50	6.5	385	004214	11	81	7.4	891
	25	004215	2.2	24	11	53	004216	4.5	27	6.0	122
	26	004219	7.7	53	6.9	408	004220	11	81	7.4	891
	27	004222	4.3	33	8.3	142	004223	7.9	51	6.5	403
	28	004226	7.8	53	6.8	413	004227	11	77	7.0	847
	29	--*					004228	2.0	27	13	54
	30	004229	2.1	25	12	53	004230	4.3	33	7.7	142

* Failed on first test pulse.

Table 7

Summary of laboratory test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C4; positive	31	004304	100	32							
pulse on TTL	32	004308	100	36							
output with	33	004312	100	33							
TPD in place.	34	004316	100	29							
	35	004320	100	29							
	36	004324	100	33							
	37	004328	100	33							
	38	004404	100	32							
	39	004408	100	36							
	40	004412	100	40							

Table 8
Summary of laboratory test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C1; negative pulse on TTL input.	41	---					005001	2.1	67	32	134
	42	---					005101	1.9	81	43	154
	43	---					005102	1.9	77	41	146
	44	---					005103	1.7	108	64	184
	45	005106	1.6	95	59	152	005201	2.1	108	51	227
	46	005109	2.0	81	41	162	005202	4.0	100	25	400
	47	005203	4.2	115	27	483	005204	6.5	140	22	910
	48	005115	1.7	105	62	179	005205	4.0	120	30	480
	49	005206	0.95	70	74	67	005207	2.6	105	40	273
	50	005208	0.95	70	74	67	005209	2.0	105	53	210

* Failed on first test pulse.

Table 9
Summary of laboratory test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C2; negative	51	109212	130	36							
pulse on TTL	52	109216	130	36							
input with	53	005308	100	36			109217	120	36		
TPD in place.	54	005311	70	32			005312	100	36		
	55	005315	70	32			005316	100	36		
	56	109604	130	40							
	57	005324	100	36			109104	110	38		
	58	005327	70	32			005328	100	36		
	59	005331	70	32			005332	100	36		
	60	005335	70	32			005336	100	36		

Table 10

Summary of laboratory test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C3; negative pulse on TTL output.	61	006002	2.1	18	8.6	38	006003	4.2	31	7.4	130
	62	005604	2.2	18	8.2	40	005605	4.5	30	6.7	135
	63	005607	2.1	16	7.6	34	005608	4.0	30	7.5	120
	64	005702	2.1	16	7.6	34	005703	3.6	23	6.4	83
	65	005705	2.2	17	7.7	37	005706	3.6	25	7.0	90
	66	005715	3.6	24	6.7	86	005716	7.5	45	6.0	338
	67	005802	2.1	16	7.7	34	005803	4.2	24	5.7	101
	68	005806	2.1	18	8.6	38	005807	3.5	25	7.1	88
	69	005810	2.1	18	8.6	38	005811	3.8	28	7.4	106
	70	005814	2.1	16	7.7	34	005815	4.2	25	6.0	105

Table 11
Summary of laboratory test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	PULSE NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C4; negative	71	008504	100			36					
pulse on TTL	72	008508	100			36					
output with	73	008512	100			36					
TPD in place.	74	008516	100			36					
	75	008520	100			36					
	76	008524	100			36					
	77	008528	100			36					
	78	008532	100			36					
	79	008536	100			36					
	80	008604	100			36					

SECTION 5.0 COMBINED ENVIRONMENT TESTS

5.1 TEST FACILITY AND EXPERIMENTAL CONFIGURATION

The combined environment tests were conducted at DNA's Blackjack 3 facility over a 4-week period from 16 February 1981 to 14 March 1981. This facility is operated by Maxwell Laboratories, Inc., in San Diego, California. A complete description of facility operating characteristics and support capabilities is given in Reference 8.

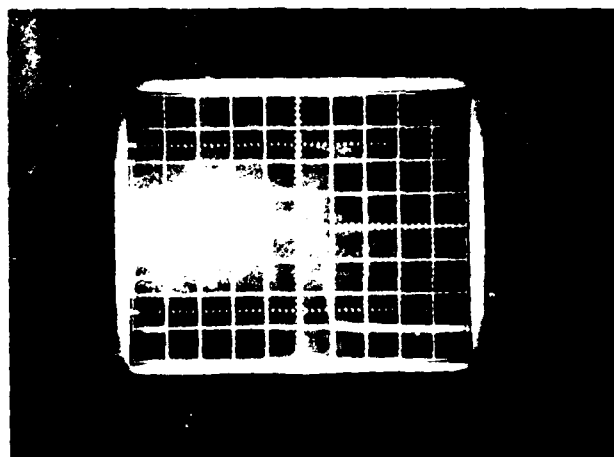
The test circuit enclosure and pulser enclosure were oriented and positioned as shown by Figure 12 to get the maximum uniform dose on the test circuits (Figure 8) and pulser active region (Figure 4). The experimental goal was to obtain 5000 rads(Si) in the test circuits



Figure 12. Orientation of test packages at Blackjack 3.

and 1000 rads(Si) in the pulser; however, it was recognized that these prompt dose levels might not be achievable in Blackjack 3 since the enclosures had not been designed specifically for this facility.

The instrumentation cables shown in Figure 12 were routed through the 4-inch diameter solid conduit which runs from the exposure region to the shielded instrumentation room. Approximately 90-foot lengths of RG-214/U were used for both signal and bias cables. The pulse response for this cable length and type was checked by observing pulses transmitted from the block house to the screen room; typical results are illustrated in Figure 13.



S_V : 1 V div

S_H : 20 ns div

Figure 13. Pulse response of instrumentation cable.

Because of the need to position the experiment enclosures very close to the bremsstrahlung source region (actually within the cylindrical portion of the machine access door as shown in Figure 12), it was not possible to use a Faraday cage as recommended by many flash x-ray test facilities. Moreover, it was not feasible to shield the exposed cable ends between the test enclosures and conduit because of the necessity to disconnect all cables and remove test enclosures (to

provide access to test ICs and TPDs) after each shot. However, these limitations did not result in an excessively noisy experimental configuration for the current and voltage measurement levels of interest.

Bias supplies (5V for ICs, 30V for PIN detector and 10 kV for charged-line pulser) and recording oscilloscopes (two Tektronix Model 7844s) were located in the facility screen room and operated in close coordination with facility diagnostic instrumentation. The recording oscilloscopes were triggered by a facility fiducial mark which normally precedes the prompt radiation pulse by about 150 ns.

5.2 DOSIMETRY

Experiment dosimetry was primarily a Kaman Sciences Corporation responsibility. The thermoluminescent dosimeter (TLD) system in use at KSC consists of encapsulated LiF powder, a Madison Research Model 120 BMR reader, and a J. L. Shepard and Associates Mark IV Model B CS-137 calibration source. Prior to this experiment, standard methods described in Reference 9 were used to calibrate the system in terms of rads(LiF). A conversion factor of 2.6 was then applied to convert from measured rads(LiF) to equivalent rads(Si) for the Blackjack 3 spectrum; this conversion factor is based on deposition analyses using the DTF photon transport code and a spectrum virtually identical to the calculated bremsstrahlung spectrum given in Reference 8.

As part of the facility services, Maxwell Laboratories provided calorimetric data from shots 3767, 3843 and 3844. They employ Ta calorimeters and use a factor of 20 to convert from measured cal/gm(Ta) to equivalent krad(Si). The calorimeters were positioned on the machine centerline and approximately four inches from the bremsstrahlung converter. This axial distance was selected to provide about the same spacing from the source region as the test ICs and TPDs. TLDs were distributed in close proximity to the two Ta calorimeters and exposed to very nearly the same prompt dose. Table 12 is a comparative summary of calorimetry and TLD results; these

Table 12
Results of calorimetry shots.

SHOT NO.	FACILITY CALORIMETRY		KAMAN TLD rads(Si)
	cal/gm(Ta)	rads(Si)	
3767	0.18	3600	4250 3550
3843	0.182	3640	3250
	0.169	3380	4200
			3900
			4650
			3900 4600
3844	0.176	3520	3625
	0.172	3440	3350
			3750
			4150
			3950 3450

data are in excellent agreement and provide a sound basis for reliance on the TLD data which were acquired throughout the test series.

Approximately 100 TLDs were irradiated during the series of 68 data shots. The pattern and locations were varied in order to examine shot-to-shot repeatability and spatial variation over the test ICs and pulser SCR assembly. Complete results are given in Table 13 for the test circuit measurements and in Table 14 for the pulser measurements. TLD location terminology is as defined by Figure 14 where the outermost locations coincide with the boundary of the active test region of each circuit board; the pattern is relative to a viewer facing the machine output.

In addition to LiF TLD and Ta calorimetry, a PIN diode signal was recorded on each shot to monitor the radiation pulse shape. This dose rate detector was supplied by KSC and located in the pulser enclosure directly behind the SCR stack assembly. The intent was to monitor

Table 13
Test circuit TLD readings.

SHOT NO.	TLD LOCATION	DOSE IN rads(Si)	SHOT NO.	TLD LOCATION	DOSE IN rads(Si)
3768	U	2450	3801	U	3200
	L	1775		L	2575
				Rt	2825
3771	U	2700		Lt	3000
	L	2300		C	3100
3772	U	2250	3804	ULt	2375
	L	1925		URt	2075
3773	U	2475		LLt	1975
	L	1900		LRt	1600
				C	2250
3777	U	2775	3807	C	3750
	L	2125		C	3425
				C	3200
3778	U	3350	3810	C	3275
	L	2500		C	3250
3782	U	2575		C	3275
	L	2150	3812	C	2900
3788	U	3425		C	2925
	L	2850		C	2750
3793	U	2925	3817	Lt	2425
	L	2625		C	2200
				Rt	2025
3796	U	2675	3821	U	3275
	L	2650		C	2900
3798	Rt	2575		L	2675
	Lt	2850	3824	Lt	3050
3799*	U	6100		C	2700
	L	4300		Rt	2550
	Rt	3700	3828	C	2700
	Lt	--		C	2500
	C	7100		C	2650
			3838	Lt	2775
				C	2975
				C	2750
				Rt	3100

* No kevlar on this shot;
one damaged TLD.

Table 14
TLD readings for pulser SCR assembly.

SHOT NO.	TLD LOCATION	DOSE IN rads(Si)
3768	U	515
	L	743
3769	U	601
	L	677
3770	U	495
	L	482
3785	Rt	440
	Lt	780
	L	525
3789	Rt	340
	Lt	330
3840	ULt	825
	URt	835
	LLt	790
	LRt	845
3815	ULt	825
	URt	743
	LLt	1089
	LRt	1106
3841	ULt	776
	URt	792
	LLt	1188
	LRt	1040
3842	ULt	1491
	URt	1411
	LLt	1331
	LRt	1225

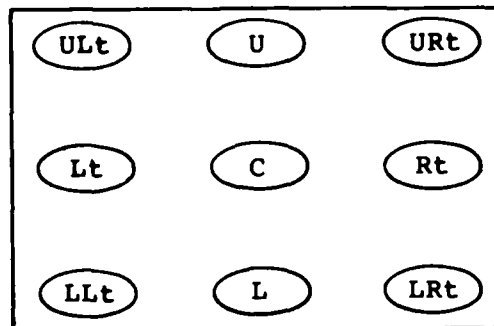
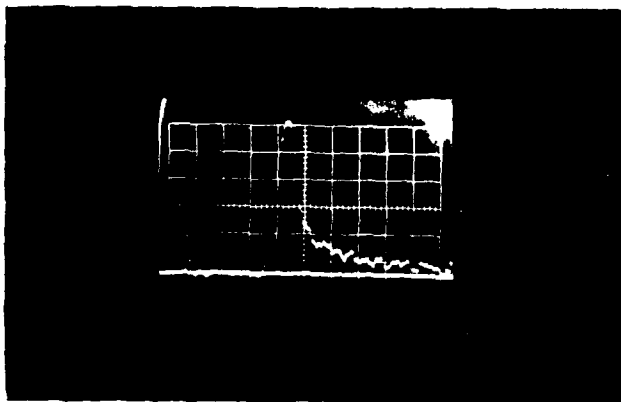


Figure 14. Identification of TLD locations.

shot-to-shot repeatability and therefore, no effort was made to calibrate this detector relative to calorimetry or TLD. Figure 15 is a selected comparison of high, nominal and low shots.

Several observations can be made from the data presented in Tables 13 and 14 and Figure 15:

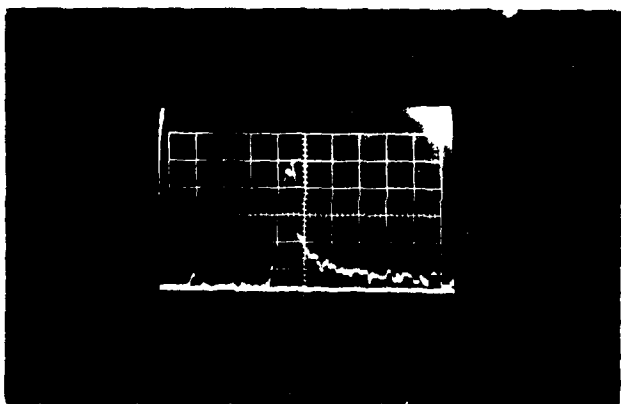
- (1) Both IC prompt dose and pulser prompt dose levels are somewhat less than the goal of 5000 rads(Si) and 1000 rads(Si), respectively.
- (2) Prompt dose output at a given location is subject to considerable shot-to-shot variation; this is probably due more to beam wander than to actual variation of machine electrical operation.
- (3) There is a noticeable dose spatial variation on both of the test boards due to the off-axis positioning of the test enclosures. The higher dose levels are on the upper portion of the test circuit board because of its position below machine centerline, and on the lower portion of the pulser SCR assembly because of its position above machine centerline.



Shot No. 3778

S_V : 0.2 A/div

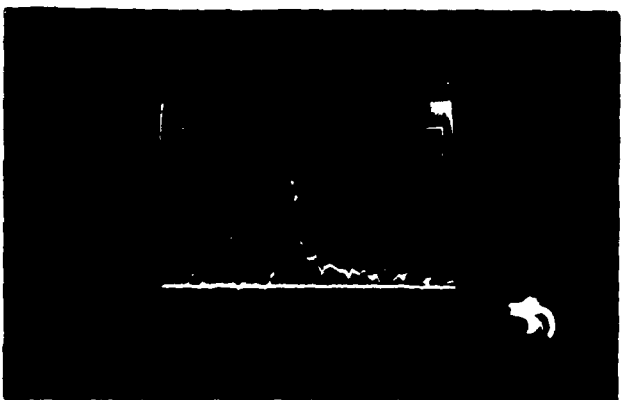
S_H : 50 ns/div



Shot No. 3833

S_V : 0.2 A/div

S_H : 50 ns/div



Shot No. 3836

S_V : 0.2 A/div

S_H : 50 ns/div

Figure 15. Typical outputs from PIN diode monitor.

- (4) Shot number 3842 was with the pulser enclosure positioned on machine centerline and about 2 inches closer to the converter; this shot was made to evaluate pulser operation for a prompt dose higher than the experiment operating level.
- (5) The PIN diode data are in general agreement with Table 14 in that these data also show that some shots may be as low as 60-70 percent of a good shot.

The overall implications of the above comments are not particularly severe in view of the objectives of the test program. The pulser functioned satisfactorily although response time would have been somewhat faster for a higher prompt dose. A prompt dose of 3500 rads(Si) is equivalent to a peak dose rate of about 7×10^{10} rads(Si)/s which is sufficient to produce intense ionization of test ICs and TPDs.

5.3 TEST PROCEDURE AND RESULTS

The 4-channel radiation-triggered pulser described in Section 3 was used for all of the combined environment testing. This pulser was designed to operate over a charging voltage range from 1-10 kV which corresponds to a current range from 10-100A into a matched 50-ohm load. High-voltage, 20 dB matched attenuators were inserted in the coaxial lines between the pulser and test circuits to extend the current range down to 1A as required for some test configurations.

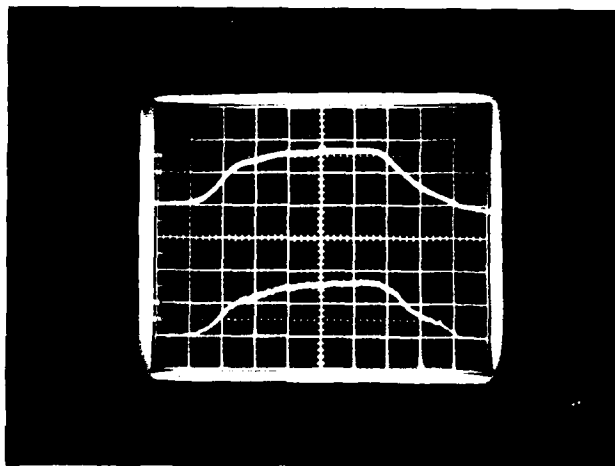
The increments of the step-stress sequence were selected to be somewhat larger than for the laboratory tests because of the need to minimize test facility time and shot requirements. It was possible to take this approach since burnout failure threshold data were already available from the baseline laboratory tests.

Eight wideband data channels would have been required to completely characterize terminal current and voltage response for the four circuits subjected to a combined environment on each test facility shot. However, because of program funding constraints and logistical problems associated with set up and operation of eight oscilloscope channels at a rental facility, the test was conducted with four data channels provided by two Tektronix Model 7844 oscilloscopes. This was not a major limitation since prior laboratory testing had demonstrated several things which relieve the requirement for complete transient response data:

- (1) Transient data are not useful for failure assessment.
- (2) Terminal voltage does not vary significantly from unit-to-unit at the same injection level.
- (3) Terminal current can in general be calculated from measured current and known operating conditions; in particular, at higher injection levels, current is a function of charging voltage only.

The four available data channels were used to record all four terminal currents, all four terminal voltages or a mixture of currents and voltages. Figure 16 is an example of terminal current data for two different test ICs, Figure 17 is an example of terminal voltage data for two different test ICs, and Figure 18 is an example of current and voltage data for the same test IC.

Toward the latter part of the test series, the test circuit configuration was temporarily modified to provide injection levels much higher than 100A. This modification consisted of summing outputs from two pulser channels into a single test terminal (referred to Figure 7, the summing point was on the test unit side of termination resistor R2 such that each charged-line pulser was still properly terminated).



Test Shot 3789

Upper Trace: Terminal Current
for Unit SN 111

S_V : 50 A/div

S_H : 20 ns/div

Lower Trace: Terminal Current
for Unit SN 112

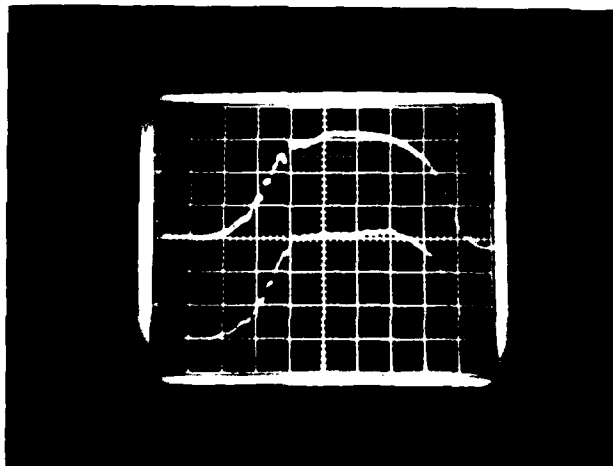
S_V : 50 A/div

S_H : 20 ns/div

Remarks:

$V_{\text{Charge line}} \approx 7 \text{ kV}$

Figure 16. Example of terminal current data.



Test Shot 3804

Upper Trace: Terminal Voltage
for Unit SN 131

S_V : 45 V/div

S_H : 20 ns/div

Lower Trace: Terminal Voltage
for Unit SN 132

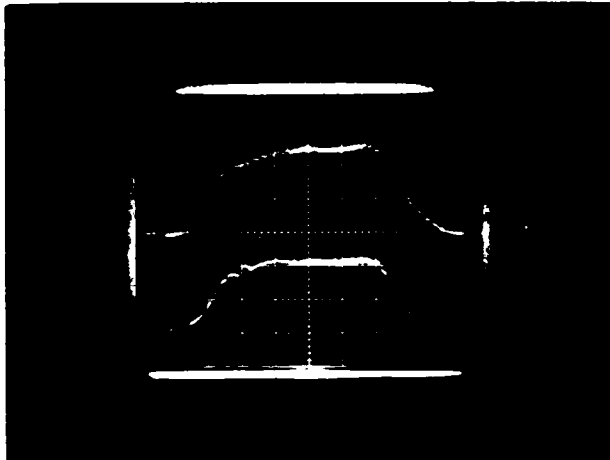
S_V : 45 V/div

S_H : 20 ns/div

Remarks:

$V'_{\text{Charge line}} \approx 850 \text{ V}$

Figure 17. Example of terminal voltage data.



Test Shot 3798

Upper Trace: Terminal Current
for Unit SN 121

S_V : 2 A/div

S_H : 20 ns/div

Lower Trace: Terminal Voltage
for Unit SN 121

S_V : 45 V/div

S_H : 20 ns/div

Remarks:

$V'_{\text{Charge line}} = 575V$

Figure 18. Example of terminal current and voltage data.

A total of 96 ICs (12 units in each of the eight test configurations described in Section 2 and depicted in Figure 2) was tested in the series of 68 good data shots. Tables 15-22 are summaries of combined environment failure data which are analagous to the laboratory data given in Tables 4-11. Because of the lack of complete transient data instrumentation, only about one-half of the tabulated current and voltage data are actual measurements; other values were estimated from very similar tests or calculated in accordance with the method outlined in Section 4. Also, as discussed in considerable detail in Section 4, failure determinations were made from electrical characterization data taken before and after each combined environment exposure. Procedures and equipment for the combined environment electrical tests were identical to those for the baseline laboratory tests.

Table 15

Summary of combined environment test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C1; positive pulse on TTL input.	117	3793	2.8*	70	25	196	3797	4.6	100	22	460
	118	3797	4.6*	100*	22	460	3802	7.5*	135	18	1012
	119	3797	4.8	100	21	480	3802	7.5*	135*	18	1012
	120	3797	4.6*	100*	22	460	3802	7.5	135	18	1012
	121	3798	4.8*	90*	19	432	3803	7.5	135*	18	1012
	122	3798	4.8	90	19	432	3803	7.5*	135*	18	1012
	123	3794	2.8	65*	23	182	3798	5.0*	100*	20	500
	124	3798	4.8	90	19	432	3803	7.5	135	18	1012
	129	3801	4.6*	100*	22	460	3804	7.5*	135*	18	1012
	130	3801	4.6	100	22	460	3804	7.5	135	18	1012
	131	3801	4.8*	100*	21	480	3804	7.5	135*	18	1012
	132	3801	4.8	100	21	480	3804	7.5	135*	18	1012

* Measured values; all others calculated or estimated from similar tests.

Table 16
Summary of combined environment test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C2; positive	105	3788	110*	35							
pulse on TTL	106	3788	110*	35							
input with	107	3788	110*	35							
TPD in place.	108	3788	110*	35							
	109	3790	110*	35							
	110	3790	110*	35							
	111	3790	110*	35							
	112	3790	110*	35							
	113	3792	110*	35							
	114	3792	110*	35							
	115	3792	110*	35							
	116	3792	110*	35							

* Measured values; all others calculated or estimated from similar tests.

Table 17

Summary of combined environment test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C3; positive pulse on TTL output.	81	3771	2.3	27*	12	62	3774	4.6	45*	9.8	207
	82	3774	4.6	45*	9.8	207	3778	9.7	65*	6.7	630
	83	3774	4.6	45*	9.8	207	3778	9.7	70*	7.2	679
	84	3774	4.6	45*	9.8	207	3778	9.7	70*	7.2	679
	85	3775	4.6	45*	9.8	207	3779	9.7	70*	7.2	679
	86	3772	2.3	27*	12	62	3775	4.6	45*	9.8	207
	87	3775	4.6	45*	9.8	207	3779	9.7	70*	7.2	679
	88	3775	4.6	45*	9.8	207	3779	9.7	60*	6.2	582
	89	3776	4.6	45*	9.8	207	3777	9.7	70*	7.2	679
	90	3776	4.6	45*	9.8	207	3777	9.7	70*	7.2	679
	91	3776	4.6	45*	9.8	207	3777	9.7	70*	7.2	679
	92	3776	4.6	45*	9.8	207	3777	9.7	70*	7.2	679

* Measured values; all others calculated or estimated from similar tests.

Table 18
Summary of combined environment test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C4; positive	93	3782	110*	35							
pulse on TTL	94	3782	110*	35							
output with	95	3782	110*	35							
TPD in place.	96	3782	110*	35							
	97	3784	110*	35							
	98	3784	110*	35							
	99	3784	110*	35							
	100	3784	110*	35							
	101	3786	110*	35							
	102	3786	110*	35							
	103	3786	110*	35							
	104	3786	110*	35							

* Measured values; all others calculated or estimated from similar tests.

Table 19

Summary of combined environment test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C1; negative pulse on TTL input.	133	---					3805	2.6*	70	27	182
	134	3805	2.6*	70	27	182	3808	3.8*	90*	24	342
	135	3805	2.6	70	27	182	3808	3.8	90	24	342
	136	3808	4.0*	100*	25	400	3810	7.0	140	20	980
	137	3806	2.6*	70*	27	182	3809	4.0	100*	25	400
	138	---					3809	2.6	70	27	182
	139	3809	4.0	90*	23	360	3810	7.0*	140	20	980
	140	3806	2.6	70	27	182	3809	4.0	120*	30	480
	141	3807	2.6	70	27	182	3808	3.8	90	24	342
	142	---					3807	2.6*	70*	27	182
	143	3807	2.6	80	31	208	3809	3.8	90*	24	342
	144	---					3807	2.6*	80*	31	208

* Measured values; all others calculated or estimated from similar tests.

** Failed on first test pulse.

TABLE 20
Summary of combined environment test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C2; negative	145	3835	240*	40							
pulse on TTL	146	3835	240	40							
input with	147	3836	240*	40							
TPD in place.	148	3836	240	40							
	149	3837	240*	40							
	150	3837	240	40							
	151	3813	120	36							
	152	3813	120*	36							
	153	3814	130	36							
	154	3814	130*	36							
	155	3814	130*	36*							
	156	3814	130	36							

* Measured values; all others calculated or estimated from similar tests.

Table 21
Summary of combined environment test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C3; negative pulse on TT1 output.	169	3821	4.3*	30*	7.0	129	3824	7.5	45	6.0	338
	170	3821	4.3	30	7.0	129	3824	7.5	45	6.0	338
	171	3818	2.9*	20*	6.9	58	3821	4.5*	30*	6.7	135
	172	3824	7.5	45	6.0	338	3827	10*	65*	6.5	650
	173	3819	2.9*	20	6.9	58	3822	4.4	30	6.8	132
	174	3822	4.3*	30*	7.0	129	3825	7.5	45	6.0	338
	175	3819	3.0*	20	6.7	60	3822	4.5	30	6.7	135
	176	3819	2.9*	20	6.9	58	3822	4.5*	30*	6.7	135
	177	3820	2.9	22*	7.6	64	3823	4.4	30	6.8	132
	178	3820	2.9	22*	7.6	64	3823	4.4*	30*	6.8	132
179	3820	2.9	24*	8.3	70	3823	4.5	30	6.7	135	
180	3820	2.9	24*	8.3	70	3823	4.5*	30*	6.7	135	

* Measured values; all others calculated or estimated from similar tests.

Table 22
Summary of combined environment test data.

TEST CONFIGURATION AND DESCRIPTION	SN OF 54L04	HIGHEST PASS LEVEL					LOWEST FAILURE LEVEL				
		SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)	SHOT NO.	I avg (A)	V avg (V)	R avg (ohms)	P avg (W)
C4; negative	157	3829	240*	40*							
pulse on TTL	158	3829	240*	40*							
output with	159	3830	240*	40*							
TPD in place.	160	3830	240*	40*							
	161	3831	240*	40							
	162	3831	240*	40*							
	163	3832	240*	40							
	164	3832	240*	40							
	165	3833	240*	40							
	166	3833	240*	40							
	167	3834	240*	40							
	168	3834	240*	40							

* Measured values; all others calculated or estimated from similar tests.

SECTION 6.0 DATA ANALYSIS

As noted in the presentation and discussion of example data given in Section 4, true failure threshold of a particular test unit lies somewhere between the highest pass level and lowest failure level. The levels developed from this program are fairly widely separated because of the impracticality of employing small pulse increments in a program which encompassed almost 200 pieceparts. A straightforward average of pass and failure levels appears to be the most reasonable approximation to true failure parameters; in equation form, this procedure can be written as

$$X_{Fi} = \frac{X_{HPLi} + X_{LFLi}}{2} \quad (7)$$

where X_{Fi} is the failure parameter of interest for the i^{th} test unit.

For comparison purpose, statistical averages are of much greater significance than failure data for single test units. Mean and standard deviation parameters can be readily calculated for some of the test groups from the standard formulas

$$\bar{X}_F = \frac{\sum_{i=1}^n X_{Fi}}{n} \quad (8)$$

and

$$\sigma_{X_F} = \left[\frac{1}{n-1} \sum_{i=1}^n (X_{Fi} - \bar{X}_F)^2 \right]^{\frac{1}{2}} \quad (9)$$

where n is the number of samples in the test group under evaluation.

Table 23 gives the results of the above statistical operations on data summarized in Tables 4, 6, 8, 10, 15, 17, 19 and 21. In a few cases where equation (7) was not applicable because failure occurred on the first test pulse, the lowest failure level was used in the

Table 23
Results of statistical analyses of failure parameters.

TEST CONFIGURATION	DATA SOURCE	\bar{I}_F (A)	σ_{I_F} (A)	σ_{I_F/\bar{I}_F}	\bar{P}_F (W)	σ_{P_F} (W)	σ_{P_F/\bar{P}_F}
Positive pulse on TTL input.	Table 4	4.5	1.9	0.43	660	470	0.71
Positive pulse on TTL input with ionizing radiation.	Table 15	5.7	0.90	0.16	668	156	0.23
Positive pulse on TTL output.	Table 6	6.0	2.7	0.46	315	237	0.75
Positive pulse on TTL output with ionizing radiation.	Table 17	6.5	1.4	0.22	386	118	0.31
Negative pulse on TTL input.	Table 8	2.4	1.2	0.48	242	172	0.71
Negative pulse on TTL input with ionizing radiation.	Table 19	3.4	1.0	0.30	316	176	0.56
Negative pulse on TTL output.	Table 10	3.3	0.81	0.25	85	45	0.53
Negative pulse on TTL output with ionizing radiation.	Table 21	4.7	1.6	0.35	165	120	0.73

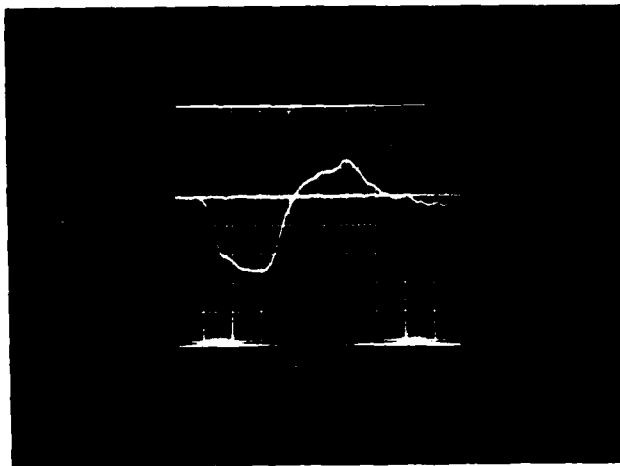
statistical calculations; this procedure would not be expected to bias the calculations significantly. For each of the four unique test conditions covered by Table 23, the data show that ICs are less susceptible to burnout in a combined environment than in a conducted current only environment. The increased tolerances are noticeable in both mean failure current and mean failure power, but the differences are not large relative to the standard deviations in these parameters.

In general, data for test configurations which included TPDs are not amenable to statistical analyses since very few or no failures were induced; observations and conclusions are still important but necessarily of a more qualitative nature. For example, consider Tables 9 and 20 for negative pulse injection on the TTL input terminal; approximately one-half of the ICs exhibited functional degradation for laboratory injection levels in the 70-100A range, whereas all 12 units passed combined environment levels up to 120A and all six of the six units tested survived a 240A injection level. In terms of the quantitative methodology represented by equation (6), the increase in TPD effectiveness is given by

$$\begin{aligned}
 DM(\dot{\gamma} \neq 0) - DM(\gamma = 0) &= 20 \log \frac{I_{TF}(\dot{\gamma} \neq 0)}{I_{TF}(\gamma = 0)} \\
 &= 20 \log \frac{\geq 240A}{\cong 100A} \quad (10) \\
 &\geq 7 \text{ dB.}
 \end{aligned}$$

For all other testing with TPDs in place, there were no failures for either laboratory or combined environment tests and hence, no basis for numerical evaluation.

TPDs may be more effective in a combined environment for the simple reason that ionized ICs are less susceptible to burnout as suggested by Table 23. It is worthwhile, however, to examine typical data to gain some further insight into the overall problem. Figure 19 shows data taken with the modified instrumentation configuration



Test Shot 3837

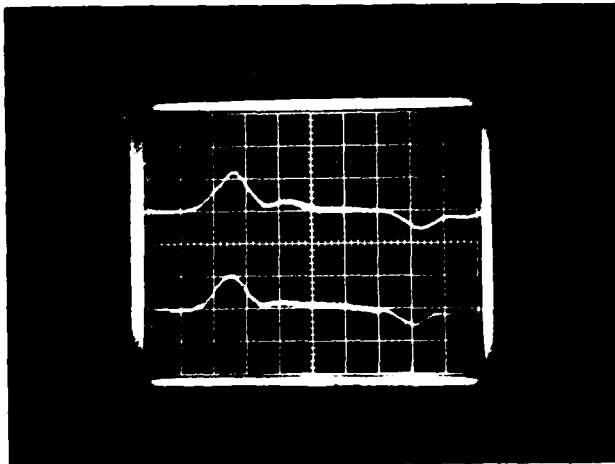
Main Trace: Terminal Current
for Unit SN 149

S_V : 100 A/div

S_H : 50 ns/div

Remarks:

$V_{\text{Charge line}} = -10 \text{ kV}$



Test Shot 3837

Upper Trace: IC Current for
Unit SN 149

S_V : 5 A/div

S_H : 20 ns/div

Lower Trace: IC Current for
Unit SN 150

S_V : 5 A/div

S_H : 20 ns/div

Figure 19. Combined environment transient data with modified pulser and test instrumentation.

(Figure 7) that provided for measurement of IC current as well as circuit terminal current. From Figure 19 and similar laboratory data presented in Figure 11, it is apparent that parasitic inductance associated with the TPD was sufficient to cause a significant voltage overshoot of the normal clamping level and a corresponding transient current into the IC under test. The significant aspect is that the resultant current pulse was narrower than the ionizing radiation pulse and consequently, the test IC would have been heavily ionized for the entire duration of the current pulse. This is in contrast to the testing performed without TPDs where the 100 ns current pulse width was about twice the radiation pulse width at half-maximum intensity. Thus, it is plausible for the difference between combined environment and laboratory failure thresholds for TPD circuit configurations to be greater than the difference between protected piecepart failure thresholds.

It is to be noted that no TPD functional degradation was noted in any of the laboratory or combined environment tests. Hence, this experimental work and related data evaluation and interpretation pertain to susceptible devices protected by TPDs rather than TPDs themselves.

SECTION 7.0

CONCLUSIONS AND RECOMMENDATIONS

This program involved development of an experimental procedure in addition to acquisition of test data. Since these objectives have considerably different evaluation criteria, program conclusions and recommendations are presented in two distinct categories.

7.1 EXPERIMENTAL PROCEDURE

The most important program conclusions pertinent to the experimental procedure are itemized in the following paragraphs:

- (1) The radiation-triggered charged-line pulser is a viable design approach. It can provide multiple output current pulses delayed by 15 ns or more from the leading edge of a prompt ionizing radiation pulse. By appropriate summing of outputs, the peak amplitude can be extended from a nominal 100A limit to several hundred amperes. A minimum dose of 1000 rads(Si) is required to effect fast, dependable operation of the SCR switches.
- (2) For pulse tests performed with a nominal 50-ohm source impedance pulser, transient data are not reliable damage indicators for even relatively simple ICs; that is, terminal current and voltage data for pulsed ICs do not show abrupt changes at the permanent damage threshold similar to what has frequently been observed for discrete, high-voltage junctions.
- (3) Permanent damage threshold is not always clearly defined from a limited set of IC electrical characterization data. There are sometimes subtle changes in dc characteristics which are indicators of incipient failure. While the subtle changes are not significant with respect to IC performance

characteristics, they are very important in that they indicate the unit under test is likely to be much more severely degraded for a subsequent pulse at the same or even lower level. It is also significant to note that the most sensitive damage indicators are not necessarily associated with the pulsed terminal.

- (4) X-ray output from the Blackjack 3 test facility is marginal for multiple unit combined environment testing unless the pulser assembly and test devices are very compactly packaged. A higher output facility such as AURORA operated by Harry Diamond Laboratories in Silver Spring, MD, Gamble II operated by the Naval Research Laboratories in Washington, D.C., HERMES II operated by Sandia Laboratories in Albuquerque, N.M., VULCAN operated by TRW Systems Group in Redondo Beach, CA., or the Model 1150 Pulserad operated by Physics International Company in San Leandro, CA., is required to achieve prompt dose levels more representative of the maximum threat for current military systems.

Recommendations in regard to experimental procedure for future similar work depend on specific program requirements. Clearly, the test facility must be carefully chosen to achieve the necessary prompt dose levels. In addition, electrical characterization must be sufficiently complete (perhaps including ac in addition to dc measurements) to detect incipient failure thresholds. It would be highly desirable to test to failure in all configurations even though this could require a capability in excess of several hundred amperes. Some consideration should be given to utilization of laboratory data to select the most susceptible test configurations, and then limiting combined environment testing to only those configurations.

7.2 TEST RESULTS

For ICs tested without TPDs, there are two significant conclusions:

- (1) Current and power failure thresholds are slightly higher for a combined environment than for a laboratory environment (that is, conducted current only) for all four test configurations (positive and negative polarity pulser on IC input and output terminals). These differences in thresholds are discernible but relatively small compared to associated standard deviations. Table 23 in the immediately preceding section provides a succinct summary of the relevant failure data.
- (2) Both current and power failure thresholds are closely grouped around respective mean values. This unusually close grouping is probably due to selection of all test ICs with the same manufacturer's date code.

Program conclusions relative to test results for TPD configurations are somewhat incomplete because of a limited number of failures; the simple terminal protection network designed especially for this program provided a comparatively high degree of IC protection. For the one test configuration (negative polarity pulse on the IC input terminal) where a few IC failures were induced, the results indicate that TPDs are more effective (by a current margin of at least 7 dB) in a combined environment than in a laboratory environment. It should be emphasized that this conclusion is based on limited data and does not have the statistical significance of the IC failure data. However, there are no data from this program to indicate unexpected responses or interactions or to suggest that TPDs are less effective in a combined environment.

A final point should be made relative to failure of ICs protected by TPDs. Practical considerations and test data strongly indicate that failure is due to test circuit parasitic elements which cause the protected IC to be subjected to severe nonideal transient conditions. Consequently, test results and conclusions are really valid only for the particular test circuits evaluated. The corollary is that if a particular system design is to be evaluated, the test article should be the candidate design including circuit layout and packaging detail.

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ATTN: R. Belt, MS-MN 17-2334
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ATTN: E. Walker
ATTN: CDOC 6/E110

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ATTN: P. Coppen

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ATTN: Dept 608

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ATTN: R. Judge

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ATTN: T. Flanagan
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Lockheed Missiles & Space Co, Inc
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Magnavox Govt & Indus Electronics Co
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ATTN: W. Bruce, MP-163
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ATTN: W. Janocko
ATTN: H. Cates
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ATTN: R. Yokomoto
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ATTN: M. Polzella, MS-D6074
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ATTN: Goodwin
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ATTN: A. Munie
ATTN: T. Ender
ATTN: M. Stich
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McDonnell Douglas Corp
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ATTN: M. Ralstein
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ATTN: Technical Library

Mission Research Corp
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ATTN: C. Longmire

Mission Research Corp
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ATTN: National Materials Advisory Board

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Raytheon Co
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Power Conversion Technology, Inc.
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ATTN: C. Kleiner
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ATTN: J. Blandford

Rockwell International Corp
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ATTN: D. Stevens

Rockwell International Corp
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Sperry Rand Corp
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ATTN: A. Witteles
ATTN: W. Willis
ATTN: W. Rowan
ATTN: Vulnerability & Hardness Laboratory
ATTN: P. Reid
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